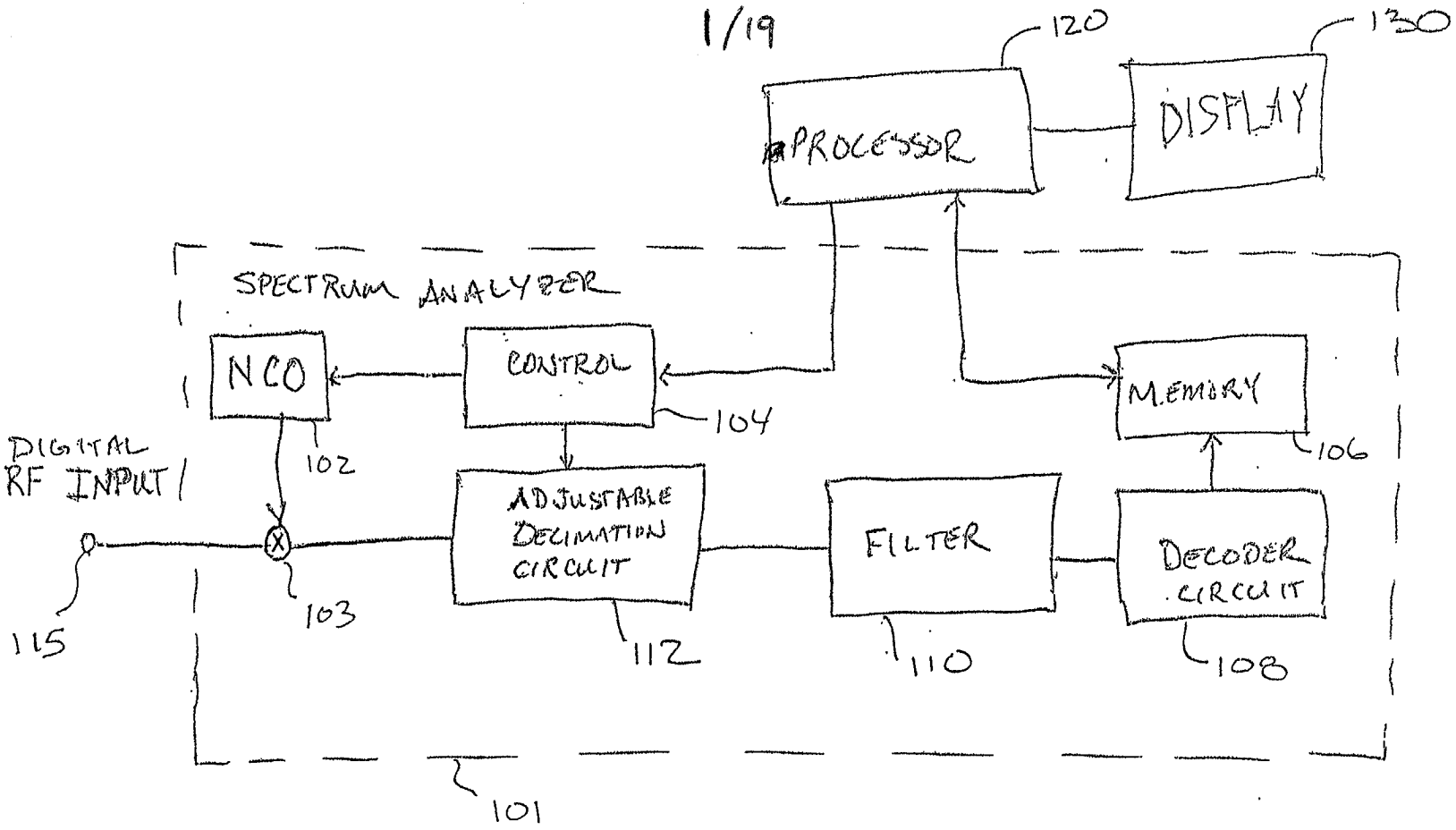
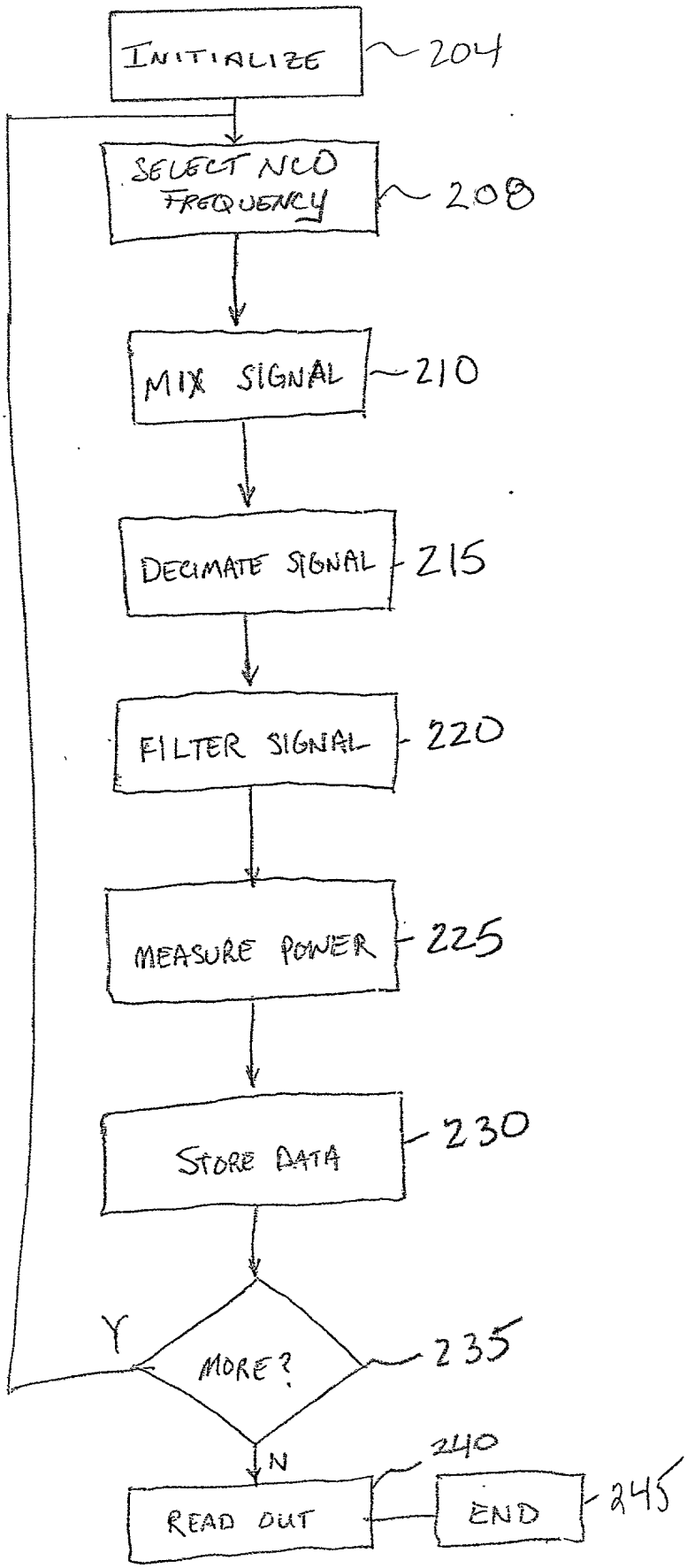

120
130
PROCESSOR
DISPLAY
SPECTRUM ANALYZER
NCO
CONTROL
104
M.EMORY
106
DIGITAL
RF INPUT
102
ADJUSTABLE
DECIMATION
CIRCUIT
FILTER
DECODER
CIRCUIT
115
103
112
110
108
101

FIG. 1

100

EFS ID: 6170280
Application No: 10025422
Document Code: DRW
Number of Pages: 1



TO2280 EGTSE660
100.226USO1

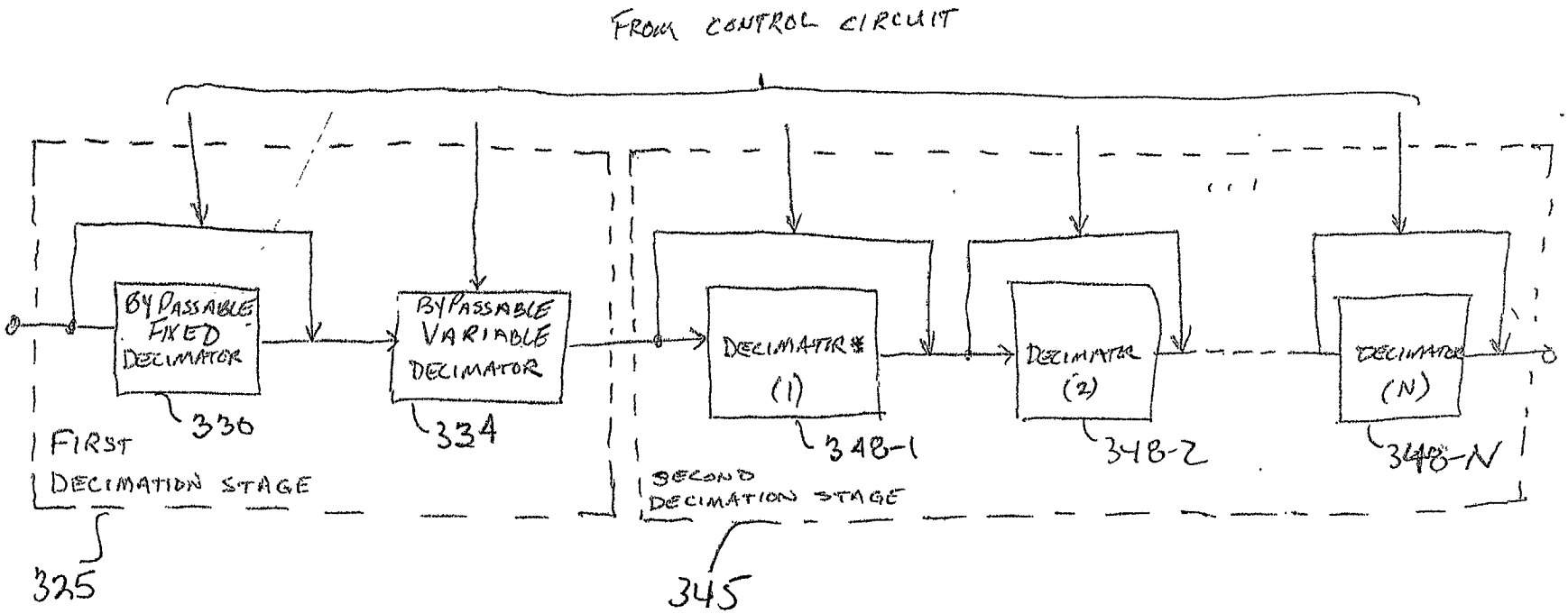


FIG. 3

300

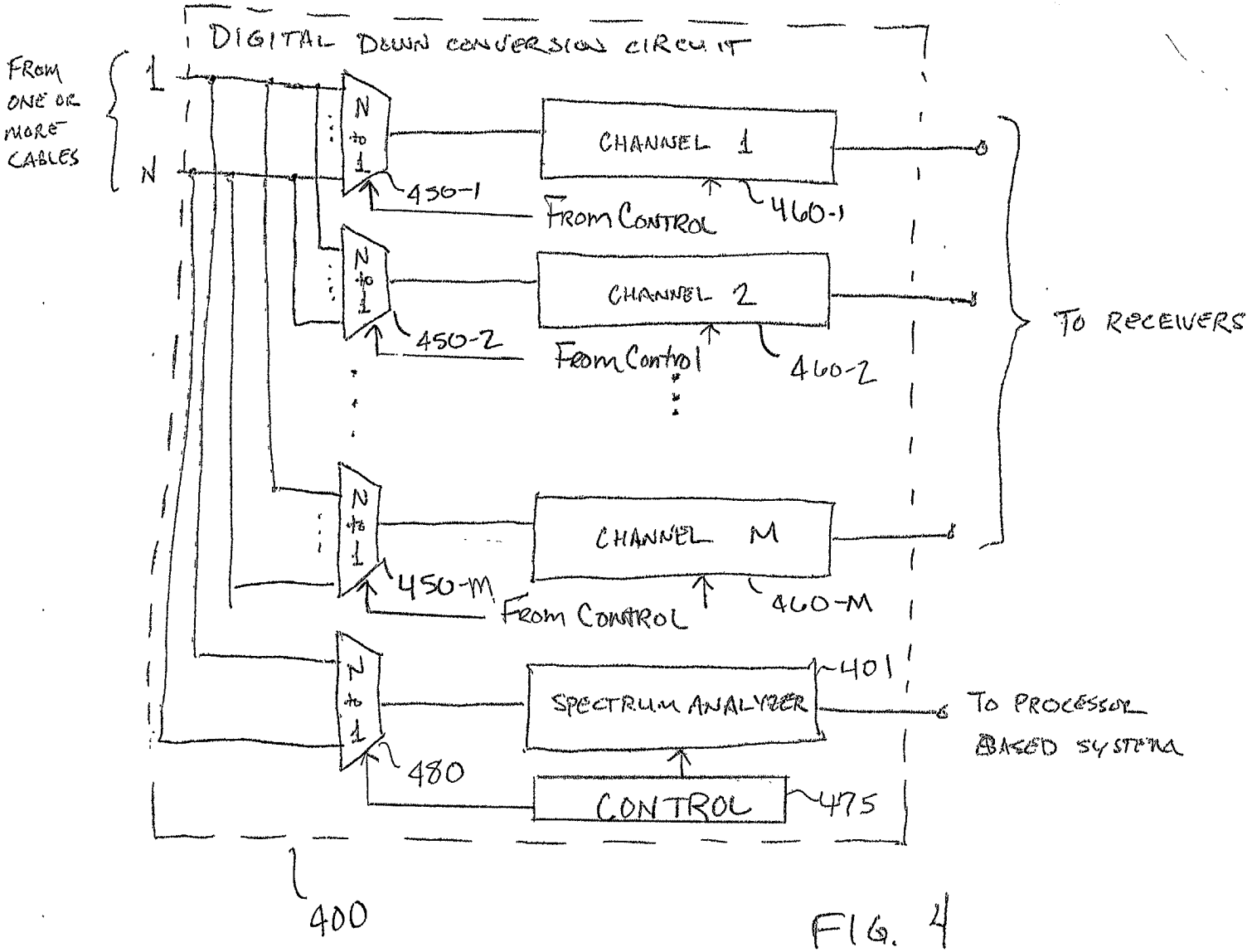

DIGITAL DOWN CONVERSION CIRCUIT
FROM ONE OR MORE CABLES
1
N
N to 1
450-1
FROM CONTROL
CHANNEL 1
460-1
450-2
FROM CONTROL
CHANNEL 2
460-2
450-M
FROM CONTROL
CHANNEL M
460-M
TO RECEIVERS
480
SPECTRUM ANALYZER
401
TO PROCESSOR BASED SYSTEMS
CONTROL
475
400

FIG. 4

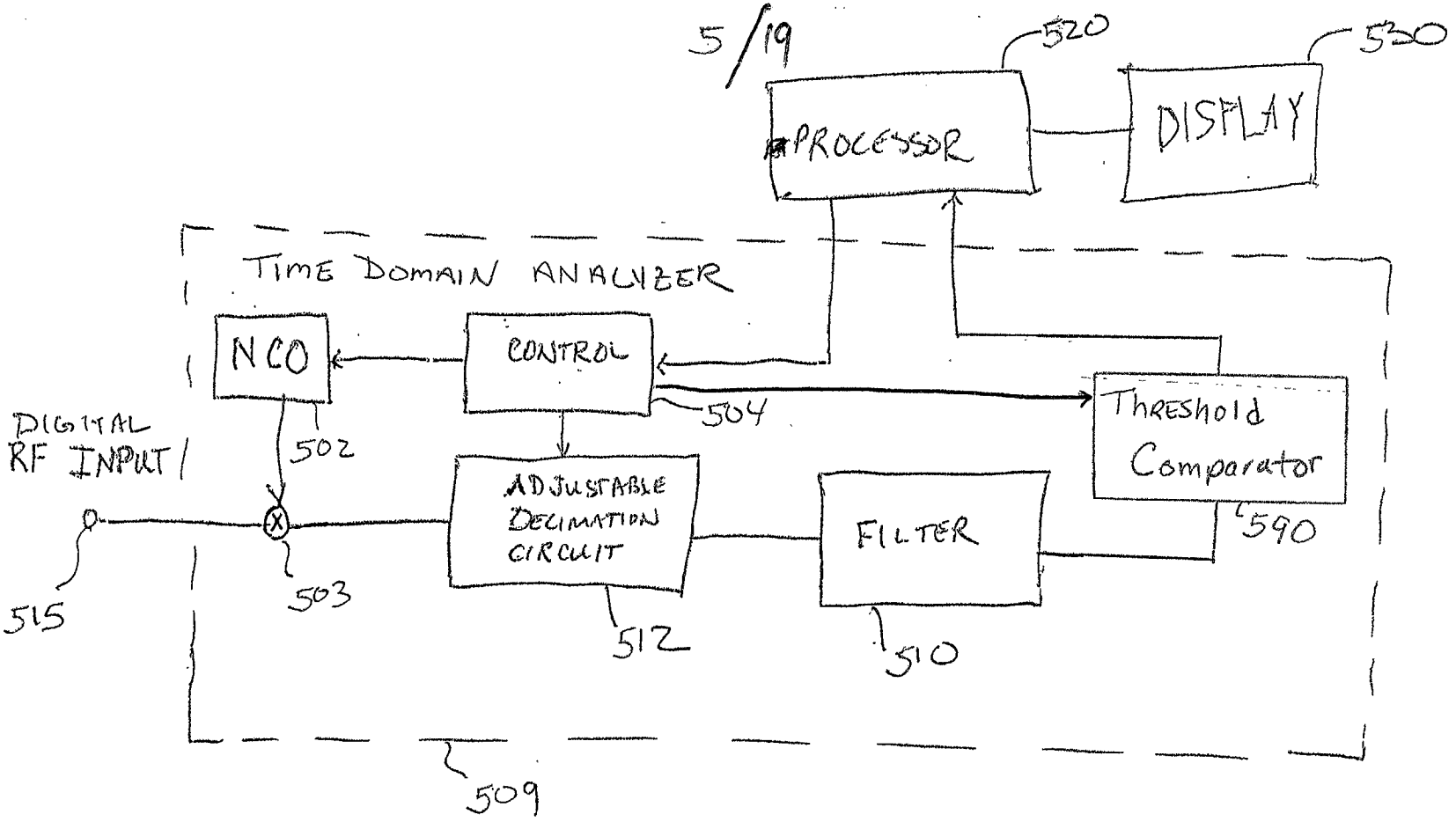

PROCESSOR
520
DISPLAY
530
TIME DOMAIN ANALYZER
NCO
CONTROL
504
Threshold Comparator
590
DIGITAL RF INPUT
502
ADJUSTABLE DECIMATION CIRCUIT
FILTER
515
503
512
510
509
500

FIG. 5

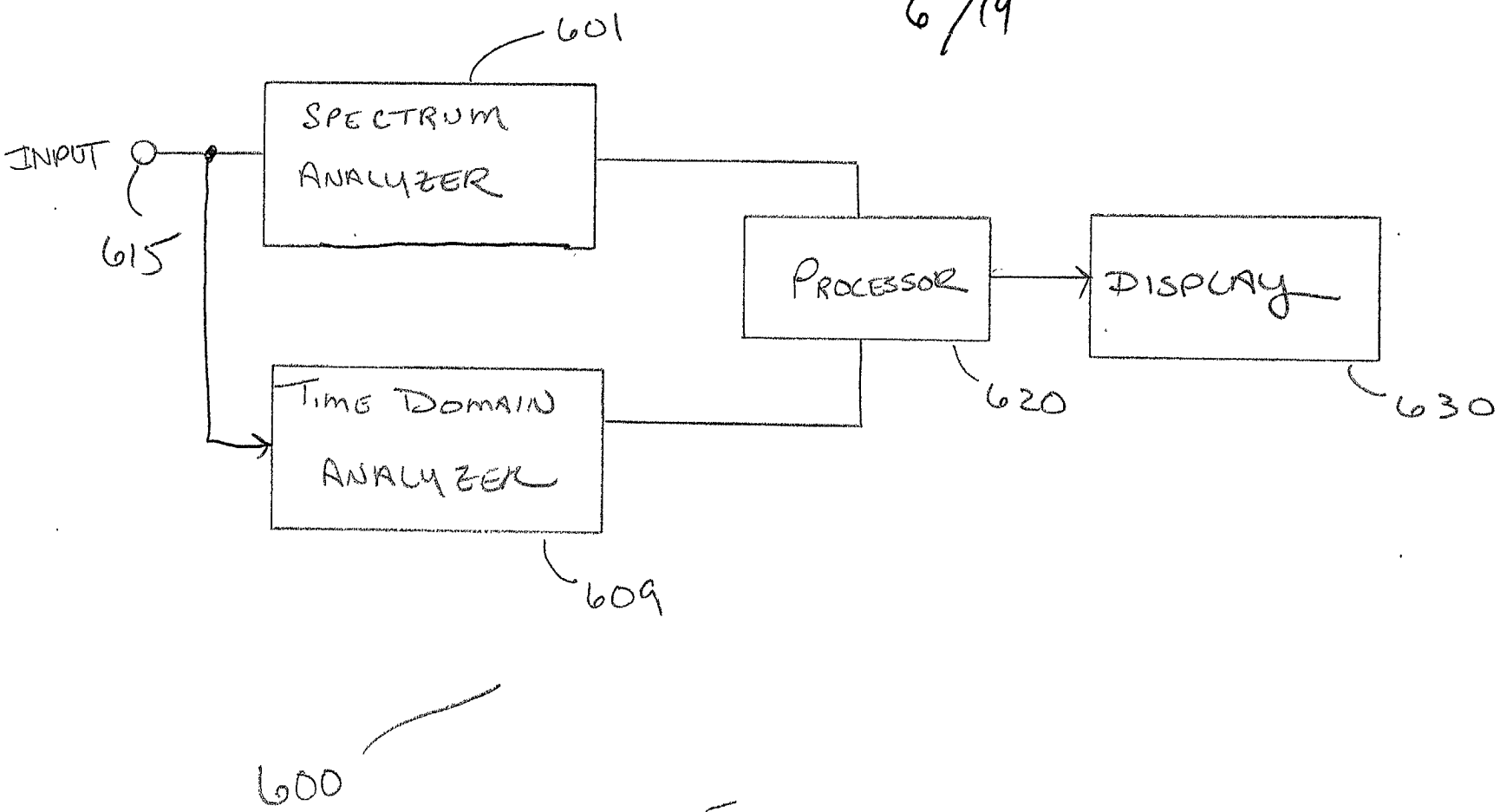

601
SPECTRUM ANALYZER
INPUT
615
PROCESSOR
DISPLAY
620
630
TIME DOMAIN ANALYZER
609
600

FIGURE 6

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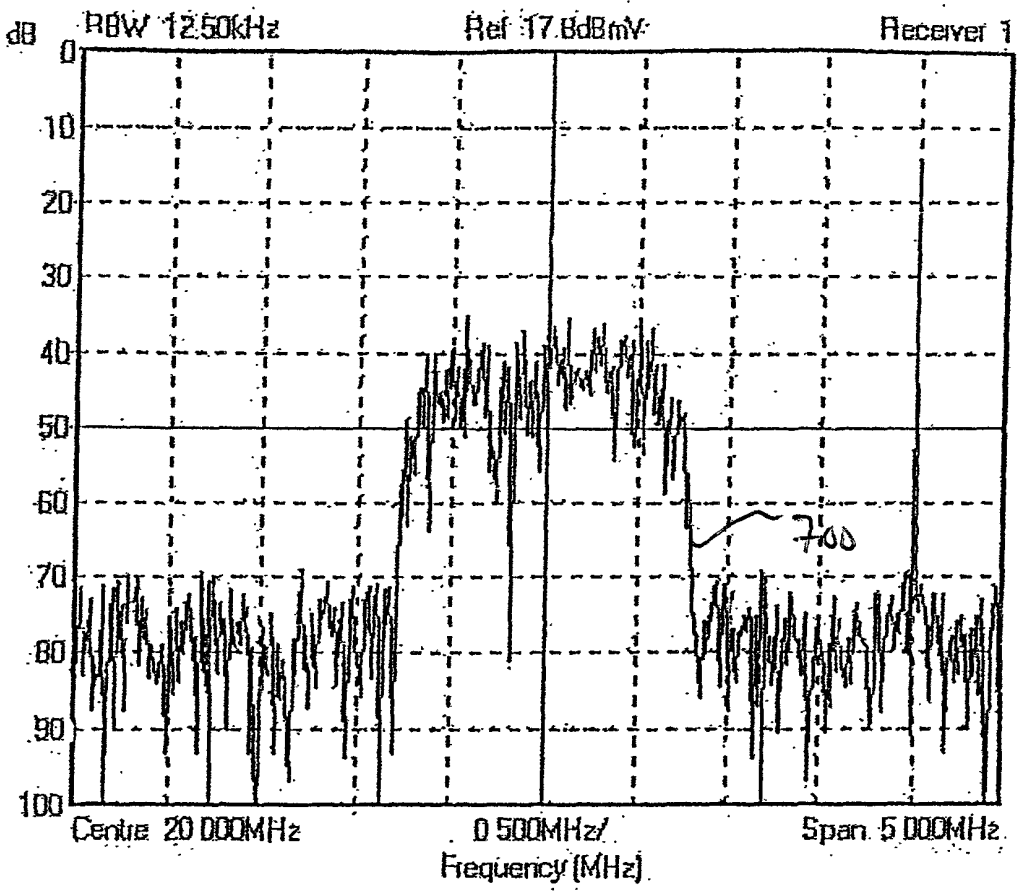

Figure 7

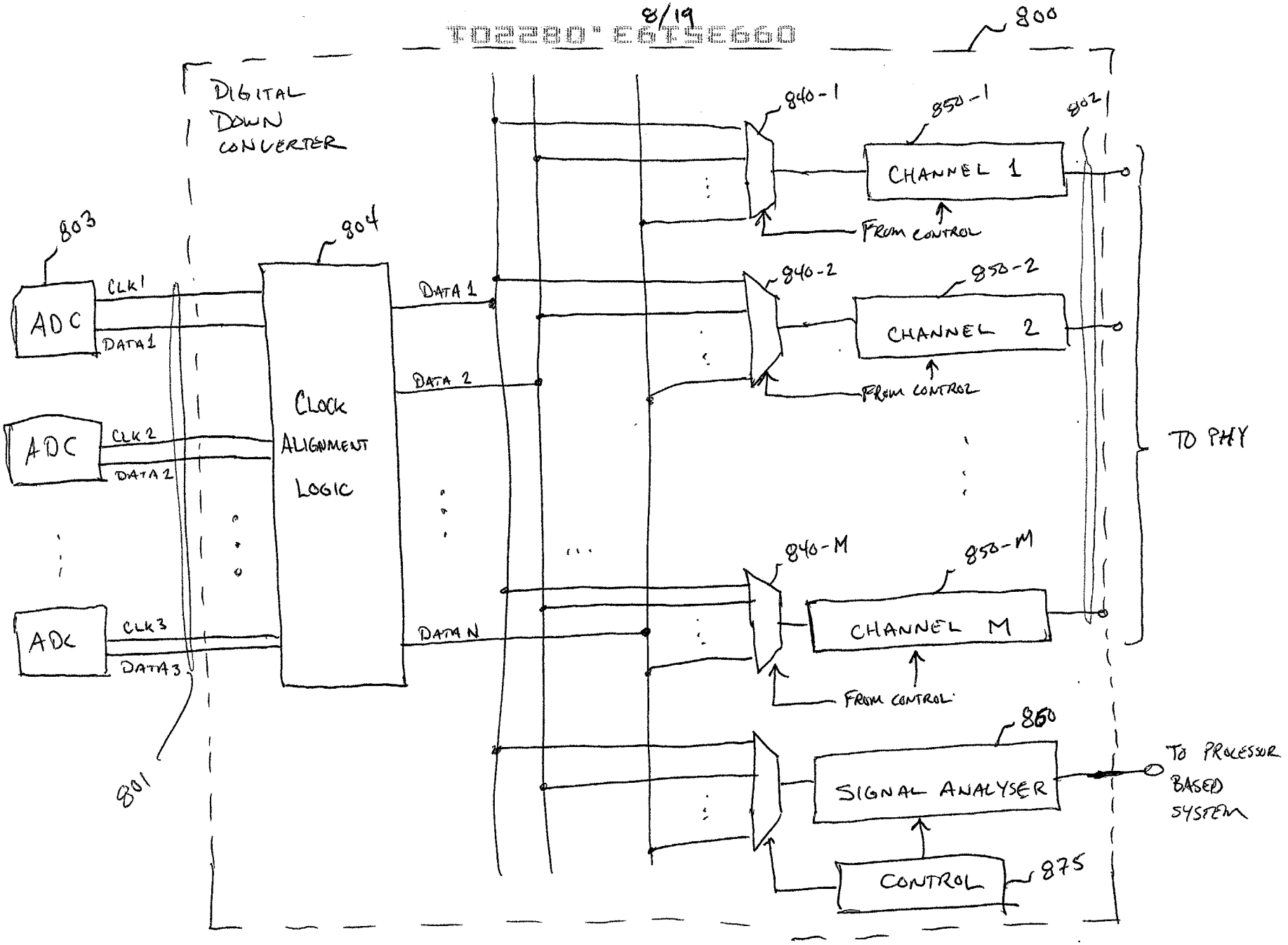
800
DIGITAL DOWN CONVERTER
803
804
ADC
CLK1
DATA1
ADC
CLK2
DATA2
ADC
CLK3
DATA3
801
CLOCK ALIGNMENT LOGIC
DATA 1
DATA 2
DATA N
840-1
850-1
CHANNEL 1
FROM CONTROL
840-2
850-2
CHANNEL 2
FROM CONTROL
840-M
850-M
CHANNEL M
FROM CONTROL
802
TO PHY
860
SIGNAL ANALYSER
TO PROCESSOR BASED SYSTEM
CONTROL
875

FIG. 8

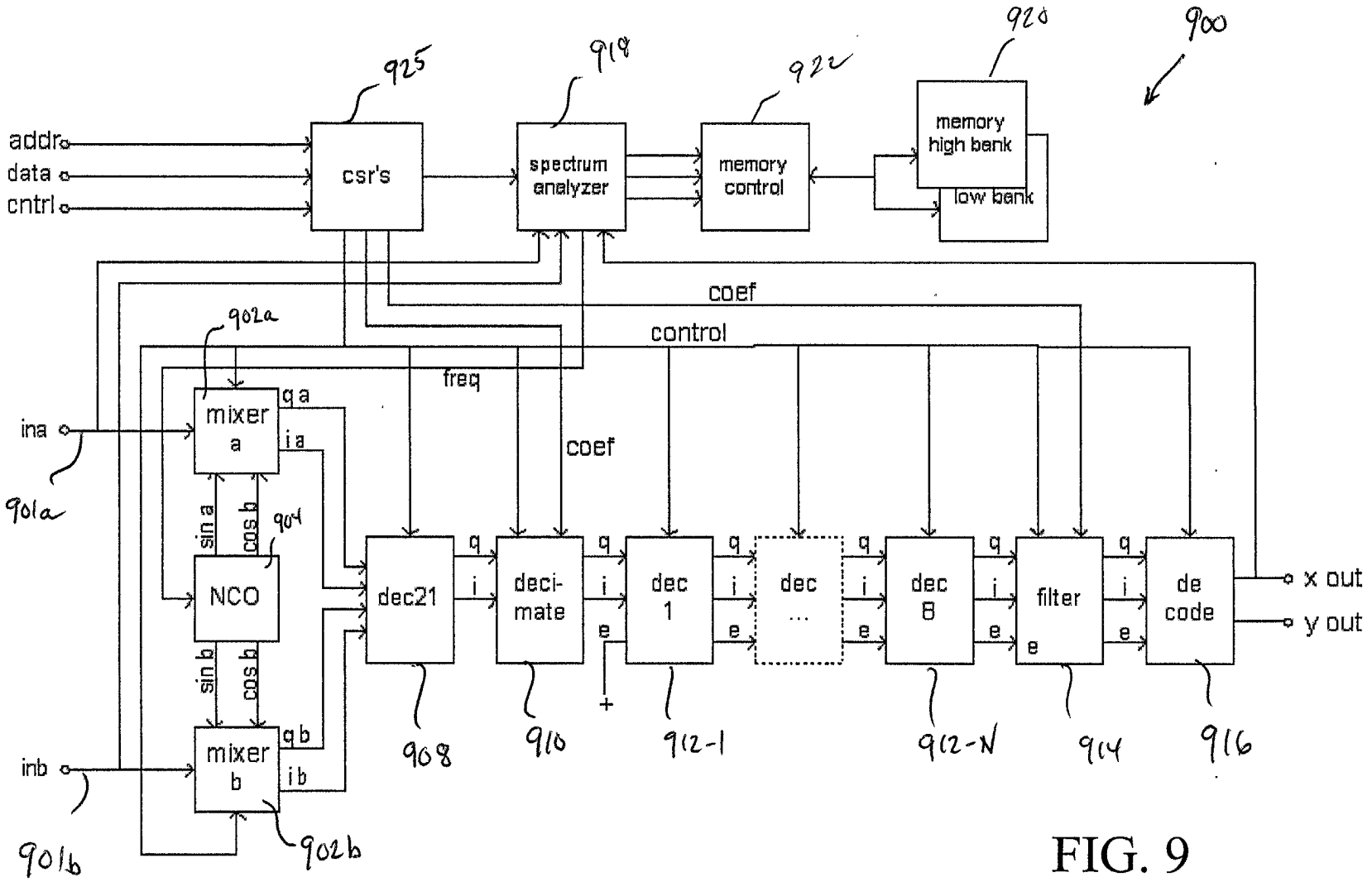
900
925
918
922
920
addr
data
cntrl
csr's
spectrum analyzer
memory control
memory high bank
low bank
coef
control
freq
902a
mixer a
qa
ia
ina
901a
sin a
cos b
904
NCO
sin b
cos b
mixer b
qb
ib
inb
901b
902b
dec21
deci-mate
dec 1
dec ...
dec B
filter
de code
x out
y out
908
910
912-1
912-N
914
916

FIG. 9

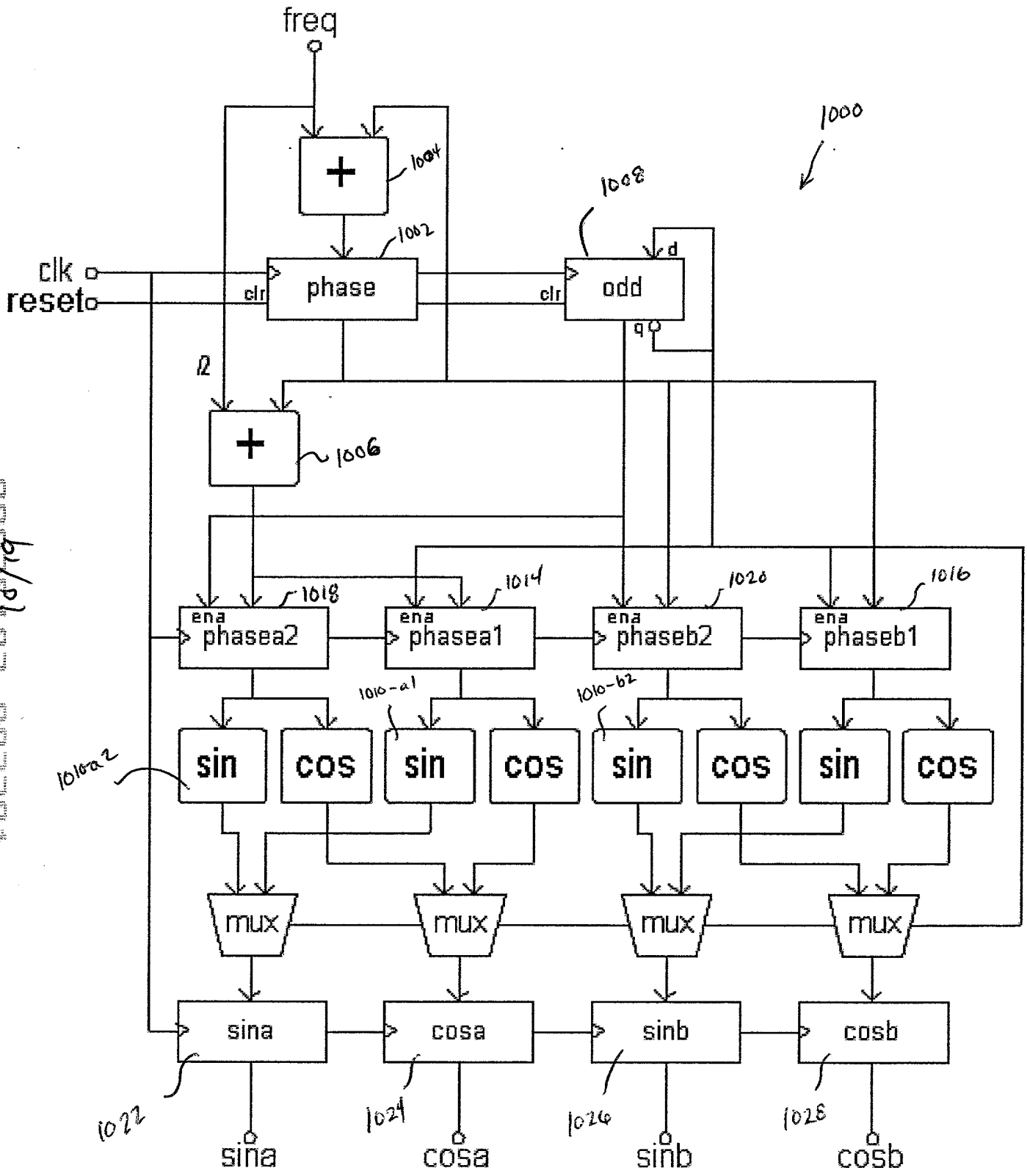
freq
1000
1004
1008
1002
clk
reset
clr
phase
clr
d
odd
q
12
1006
1018
1014
1020
1016
ena
phasea2
ena
phasea1
ena
phaseb2
ena
phaseb1
1010-a1
1010-b2
1010a2
sin
cos
sin
cos
sin
cos
sin
cos
mux
mux
mux
mux
sina
cosa
sinb
cosb
1022
1024
1026
1028
sina
cosa
sinb
cosb

FIG. 10

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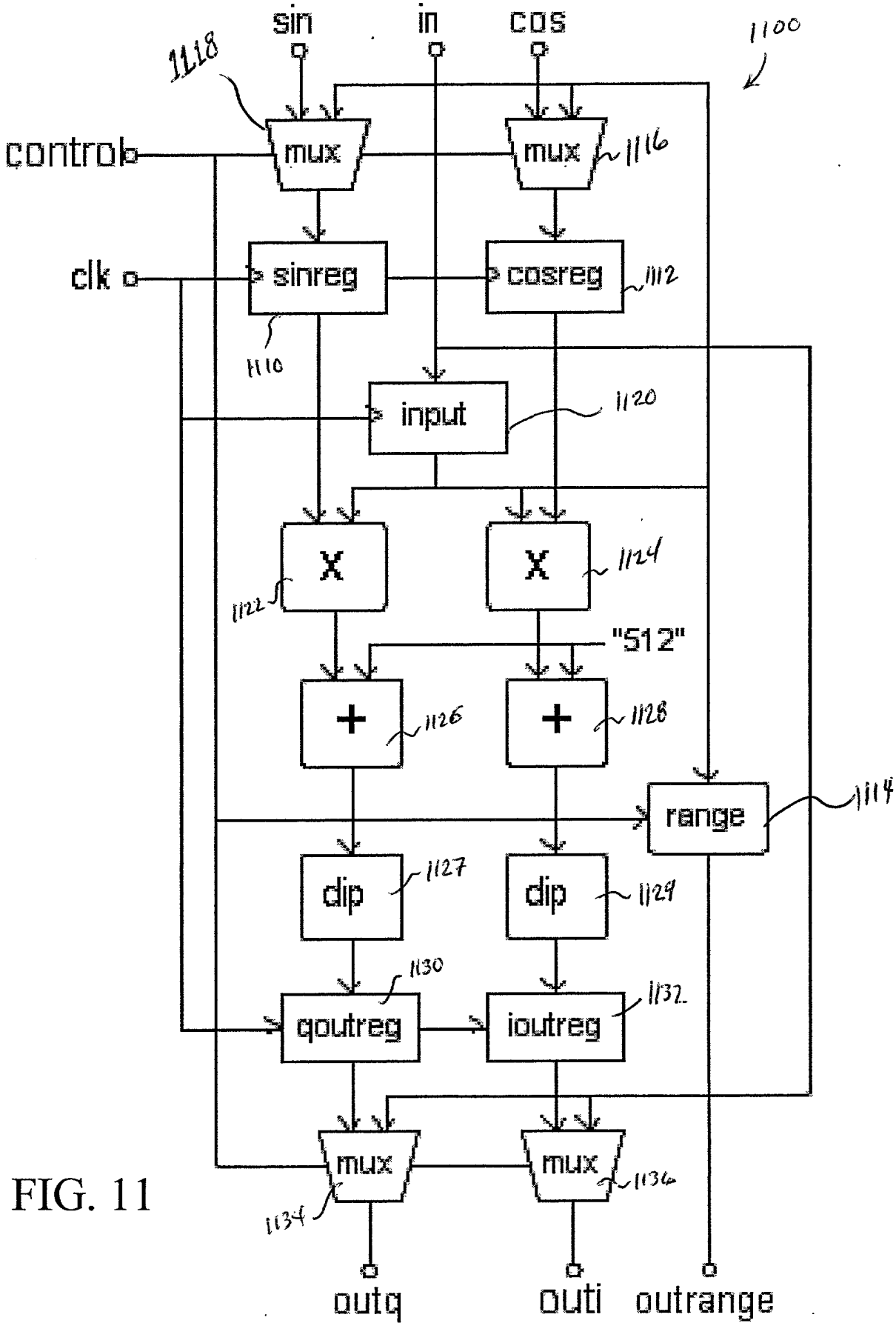


FIG. 11

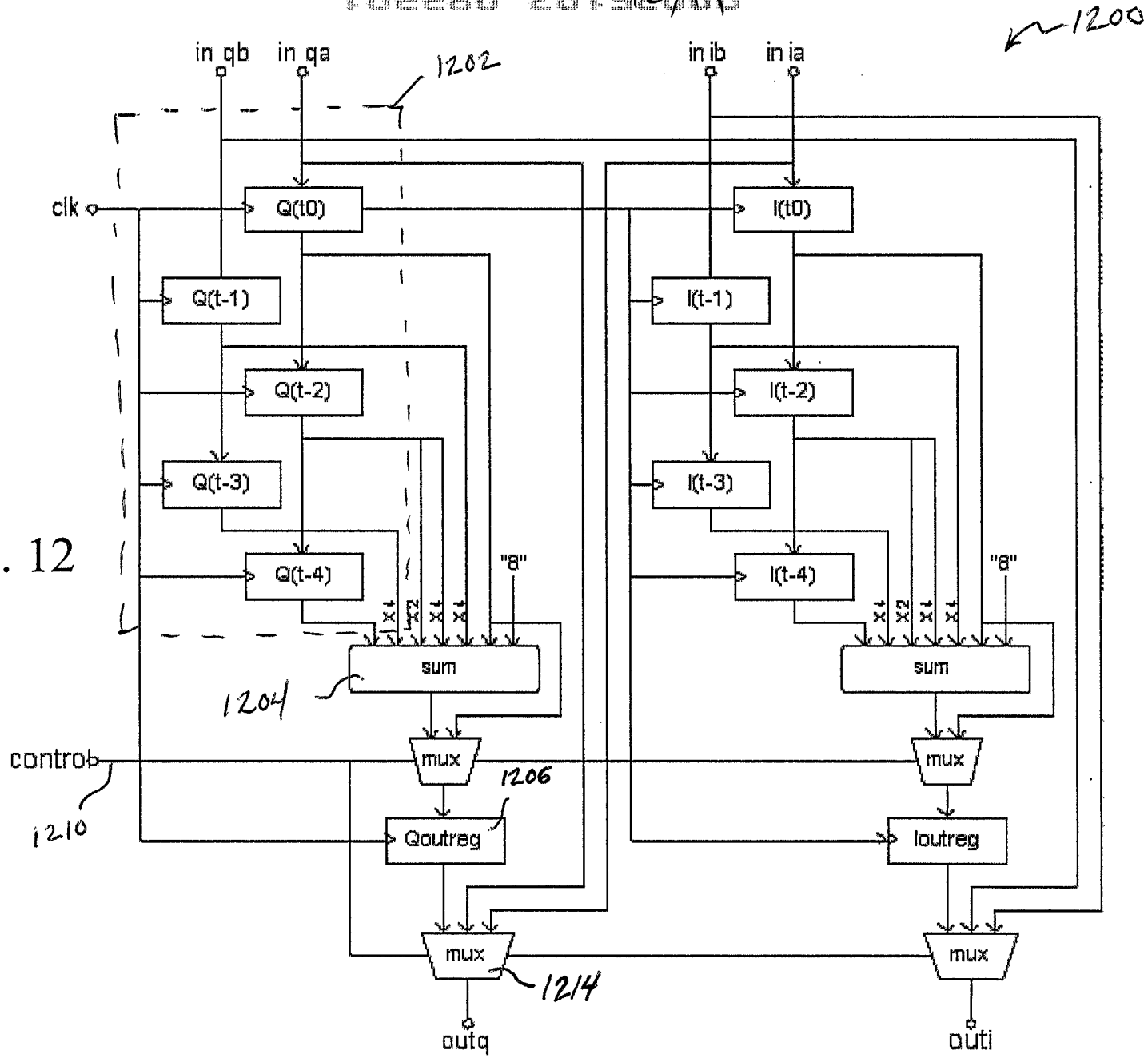
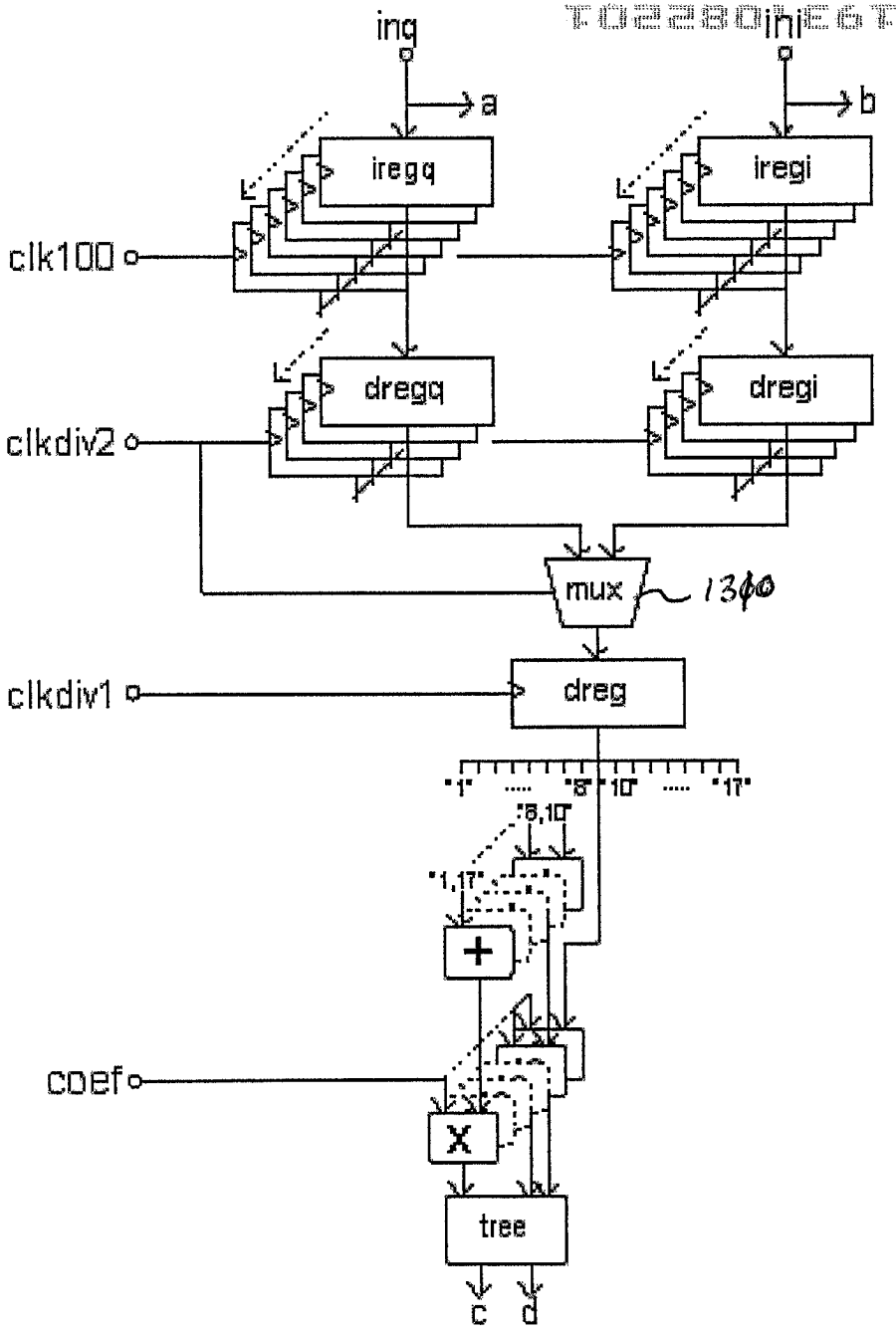

1200
1202
in qb
in qa
in ib
in ia
clk
Q(t0)
I(t0)
Q(t-1)
I(t-1)
Q(t-2)
I(t-2)
Q(t-3)
I(t-3)
Q(t-4)
I(t-4)
"8"
"8"
x4
x2
x4
x4
sum
sum
1204
control
1210
mux
mux
1206
Qoutreg
Ioutreg
mux
mux
1214
outq
outi

FIG. 12


inq
a
b
iregq
iregi
clk100
dregq
dregi
clkdiv2
mux
1340
clkdiv1
dreg
"1" ..... "8" "10" ..... "17"
"8,10"
"1,17"
+
coef
X
tree
c
d

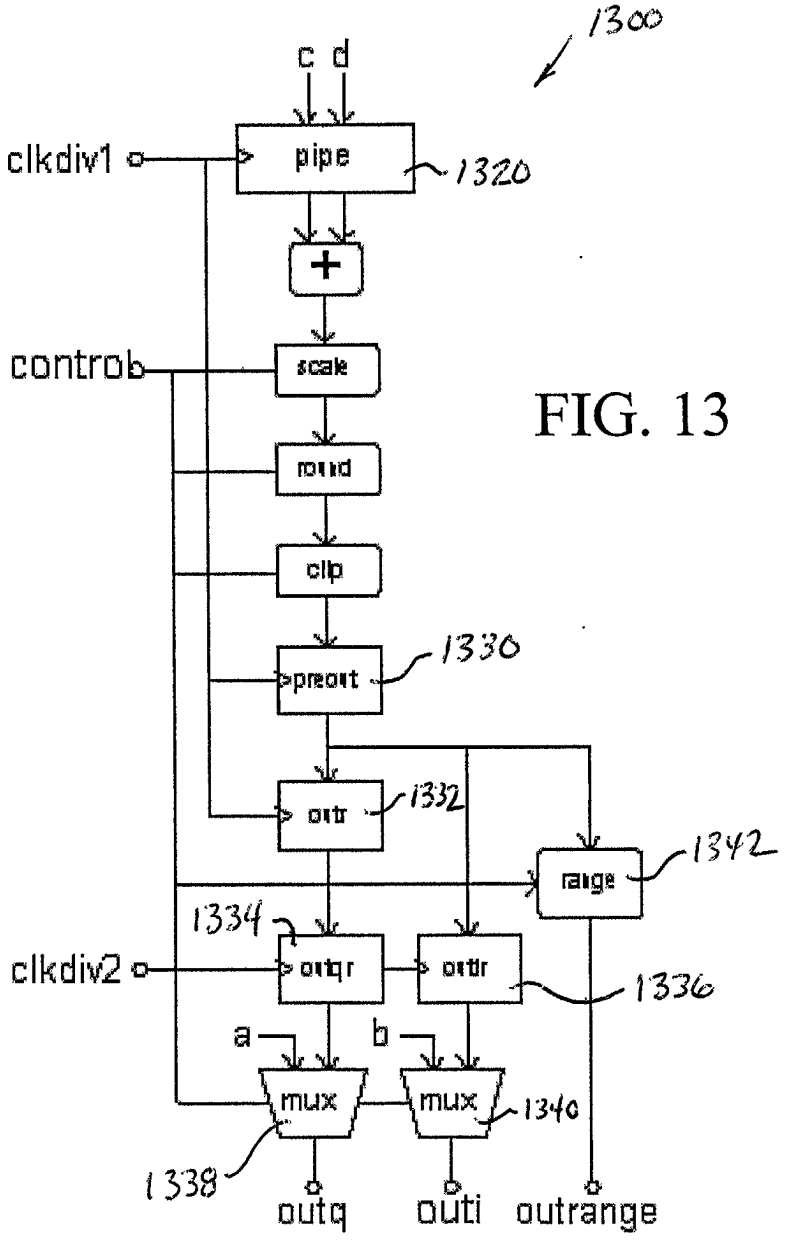

1300
c d
clkdiv1
pipe
1320
+
controb
scale
round
clip
preout
1330
outr
1332
range
1342
1334
outqr
outir
1336
clkdiv2
a
b
mux
mux
1340
1338
outq
outi
outrange

FIG. 13

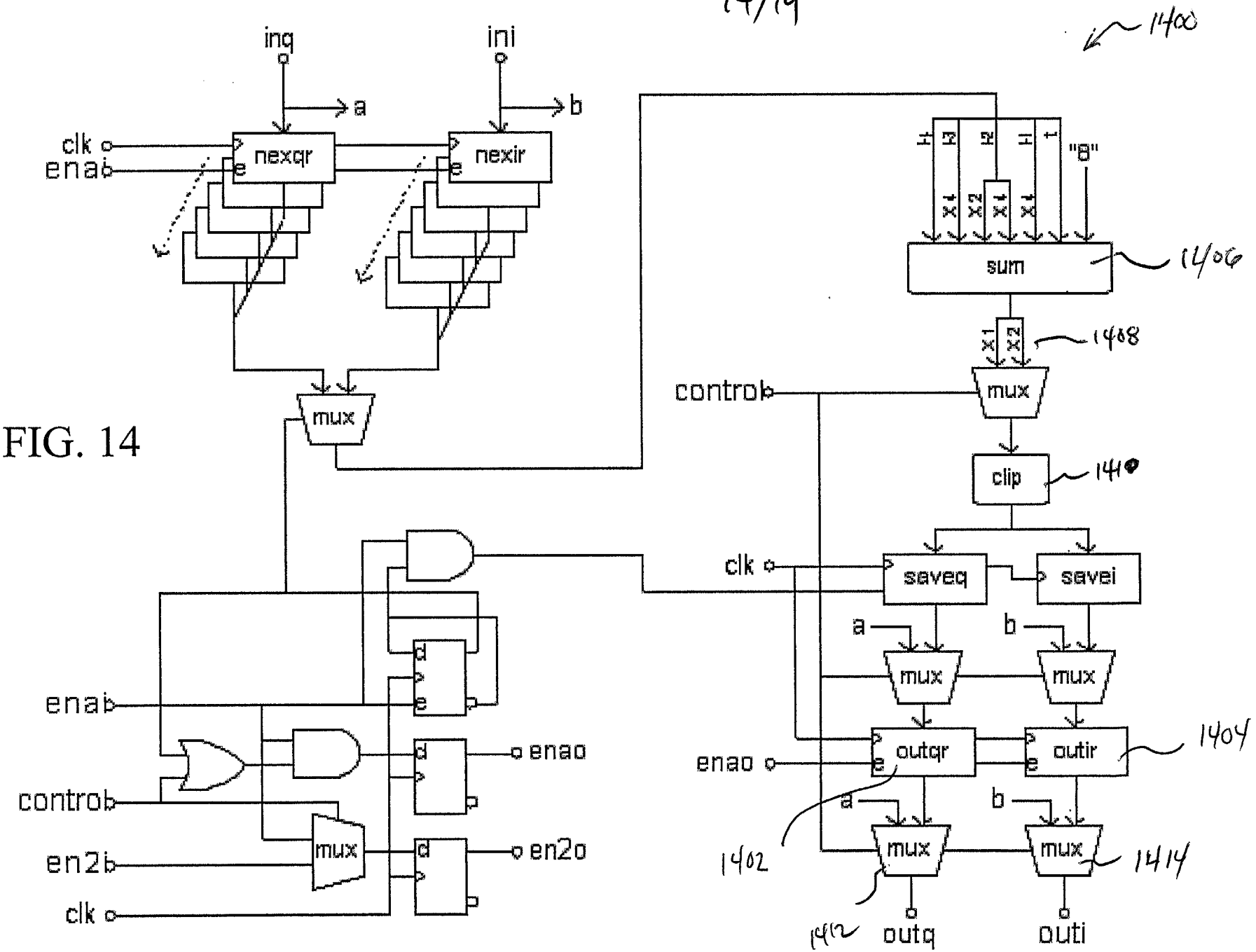

inq
ini
a
b
clk
enab
nexqr
nexir
e
mux
"8"
sum
1406
x1
x2
1408
controb
clip
1410
saveq
savei
enai
enao
outqr
outir
1404
en2b
en2o
1402
1412
outq
outi
1414
1400

FIG. 14

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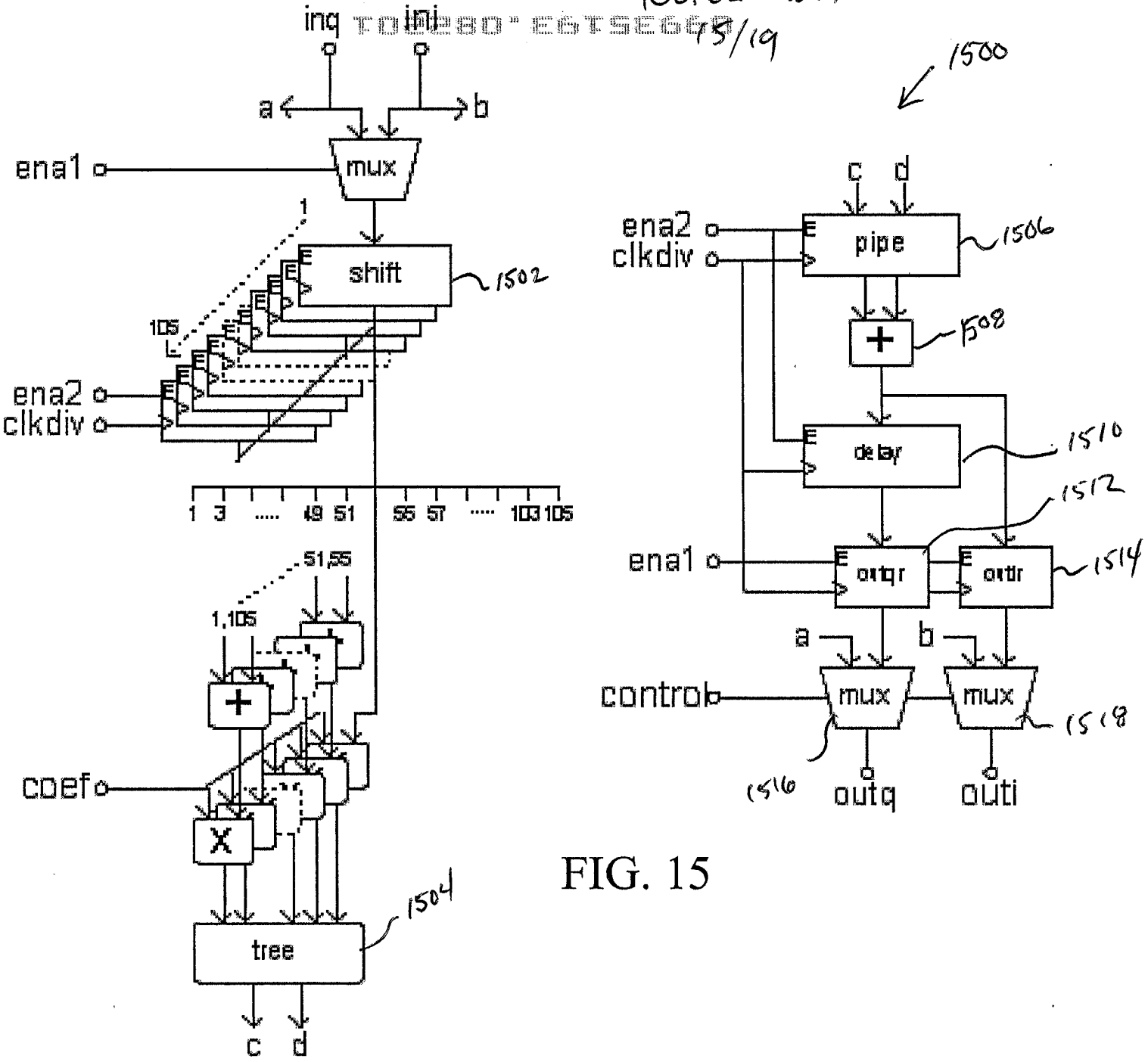


FIG. 15

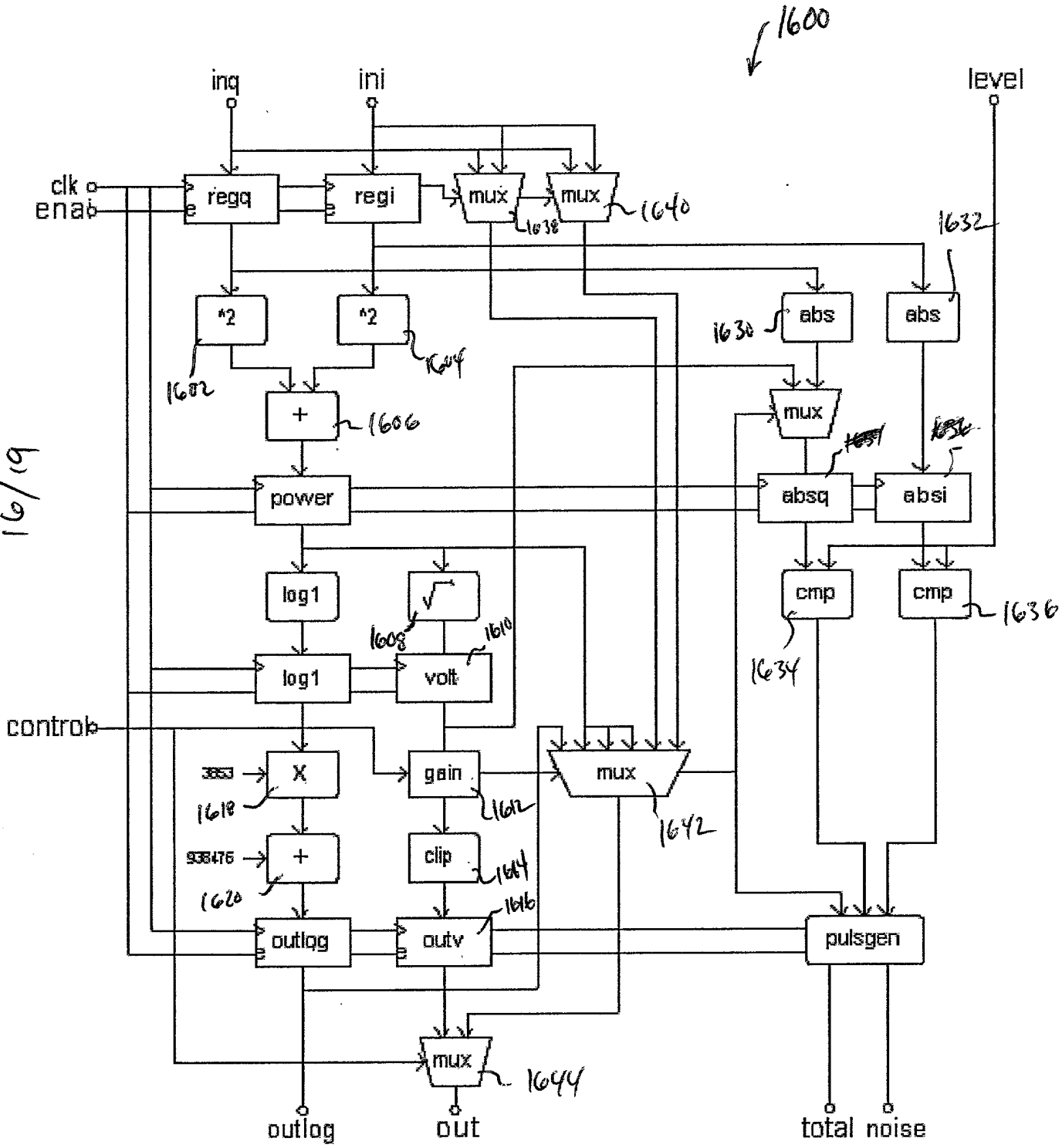

1600
inq
ini
level
clk
enab
regq
regi
mux
mux
1638
1640
1632
^2
^2
1602
1604
1630
abs
abs
+
1606
mux
power
absq
absi
log1
cmp
cmp
1636
1608
1610
log1
volt
1634
control
X
gain
mux
1618
1612
1642
+
clip
1620
1614
outlog
outv
1616
pulsgen
mux
1644
outlog
out
total noise

FIG. 16

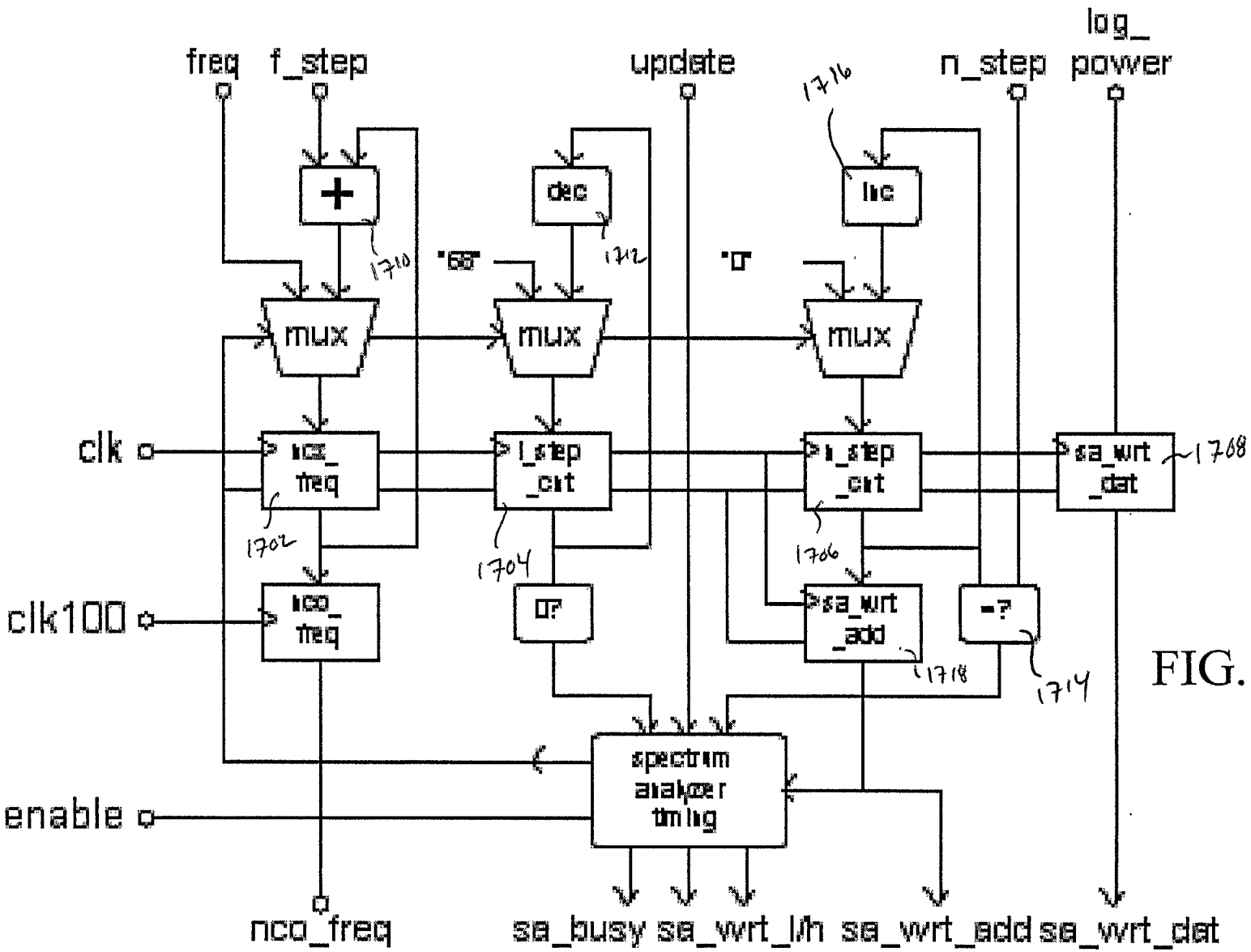

1700
freq
f_step
update
n_step
log_
power
+
dec
inc
1710
"66"
1712
"0"
1716
mux
mux
mux
clk
nco_
freq
f_step
_cnt
n_step
_cnt
sa_wrt
_dat
1708
1702
1704
1706
clk100
nco_
freq
0?
sa_wrt
_add
=?
1718
1714
spectrum
analyzer
timing
enable
nco_freq
sa_busy
sa_wrt_ldh
sa_wrt_add
sa_wrt_dat

FIG. 17

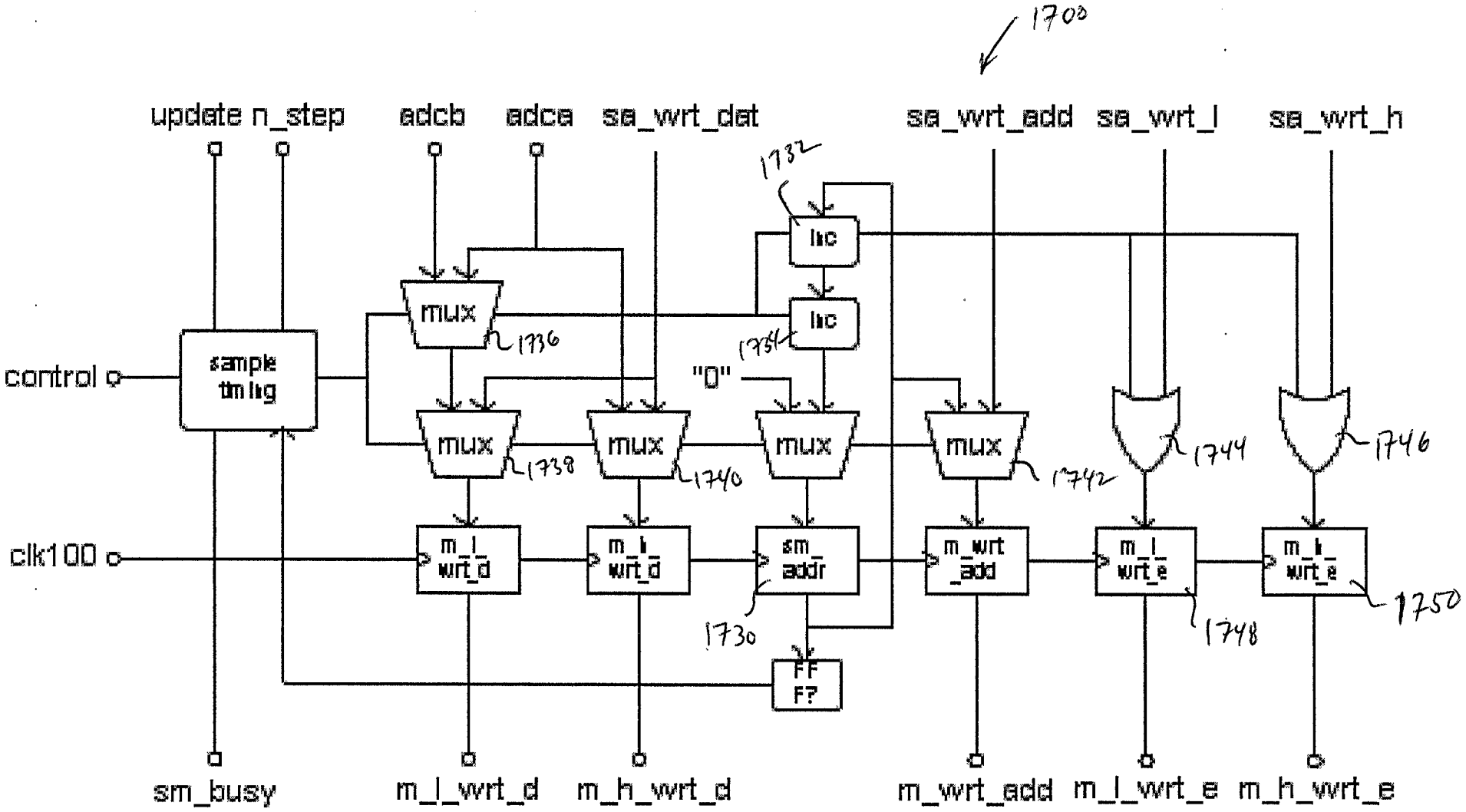
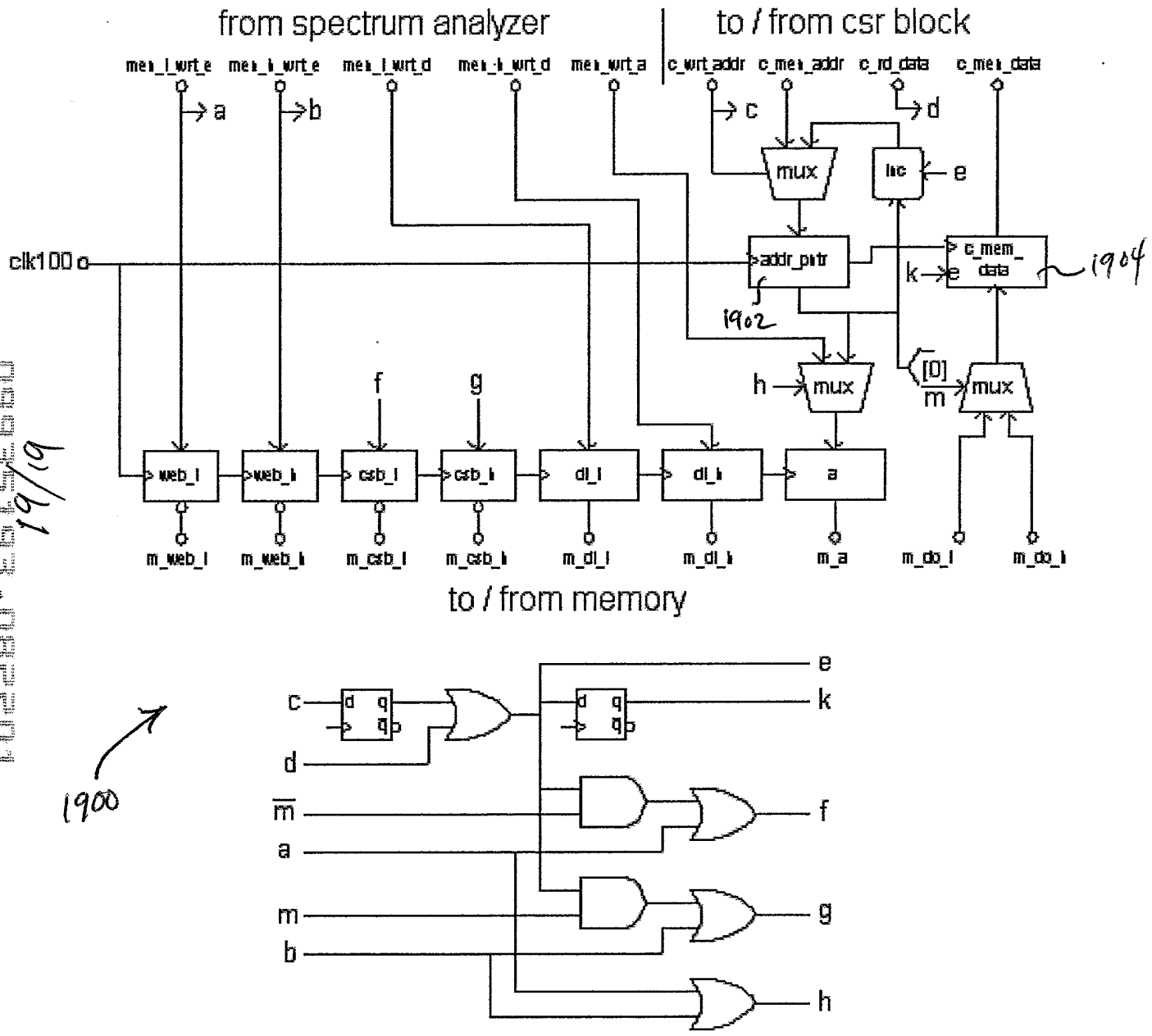

1700
update
n_step
adcb
adca
sa_wrt_dat
sa_wrt_add
sa_wrt_l
sa_wrt_h
1732
inc
inc
mux
1736
1734
"0"
control
sample timing
mux
mux
mux
mux
1738
1740
1742
1744
1746
clk100
m_l_wrt_d
m_h_wrt_d
sm_addr
m_wrt_add
m_l_wrt_e
m_h_wrt_e
1730
1748
1750
FF
F?
sm_busy
m_l_wrt_d
m_h_wrt_d
m_wrt_add
m_l_wrt_e
m_h_wrt_e

FIG. 18


from spectrum analyzer
to / from csr block
mem_l_wrt_e
mem_h_wrt_e
mem_l_wrt_d
mem_h_wrt_d
mem_wrt_a
c_wrt_addr
c_mem_addr
c_rd_data
c_mem_data
a
b
c
d
mux
inc
e
clk100o
addr_ptr
c_mem_data
1902
1904
k
h
mux
[0]
m
mux
f
g
web_l
web_h
csb_l
csb_h
dl_l
dl_h
a
m_web_l
m_web_h
m_csb_l
m_csb_h
m_dl_l
m_dl_h
m_a
m_do_l
m_do_h
to / from memory

1900
c
d
m
a
m
b
e
k
f
g
h

FIG. 19